IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended) A data transfer control circuit for carrying out data transfer by using a plurality of bus masters, comprising:

a data bus connected to a peripheral apparatus, said data bus having a plurality of unit data buses, each of which transfers data concurrently;

a plurality of bus masters connected to each of the unit data buses and configured to send a <u>bus</u> request signal requesting <u>to acquire</u> a use of each of said unit data buses, and to <u>transfer data on</u> <s>use</s> said unit data buses requested when a request by means of said <u>bus</u> request signal is granted; and

one bus controller connected to all of the bus masters and configured to split-control said unit data buses for said plurality of bus masters by giving a grant signal to the bus masters, which grants the use of each of said unit data buses in accordance with said <u>bus</u> request signal, wherein

the <u>bus</u> request signal <u>is sent to said bus controller prior to data transfer and</u> has a field comprising a plurality of bits <u>for specifying necessary bit width</u>, each of said plurality of bits identifying <s>corresponding to</s> a respective one of said unit data buses, and said bus controller grants the use of each of said unit data buses specified by the bits of said <u>bus</u> request signal.

Claim 2 (Previously Presented): The data transfer control circuit according to claim 1, wherein:

said bus controller sends the grant signal to said bus masters based on a bus release requesting signal requesting release of said unit data buses.

Claim 3 (Previously Presented): The data transfer control circuit according to claim 1, wherein:

said bus controller includes a monitor circuit for monitoring availability of said unit data buses.

Claim 4 (Previously Presented): The data transfer control circuit according to claim 3, wherein:

said bus controller judges whether said unit data buses of said data bus are available based on a monitoring result of said monitor circuit, and when said unit data buses are available, said bus controller provides the grant signal of the use of said unit data buses to said bus master.

Claim 5 (Previously Presented): The data transfer control circuit according to claim 3, wherein:

said bus controller sends a state signal indicating the availability of said unit data buses to each of said bus masters based on a monitoring result of said monitor circuit.

Claim 6 (Currently Amended): The data transfer control circuit according to claim 1, wherein:

said bus request signal includes information specifying each unit data bus in said data bus.

Claim 7 (Currently Amended): The data transfer control circuit according to claim 1, wherein:

said <u>bus</u> request signal includes information specifying the number of the unit data

buses in said data bus.

Claim 8 (Currently Amended) An information processing system for carrying out data

transfer by using a plurality of bus masters, comprising:

a peripheral apparatus;

a data bus connected to a peripheral apparatus, said data bus having a plurality of unit

data buses, each of which transfers data concurrently;

a plurality of bus masters connected to each of the unit data buses and configured to

send a <u>bus</u> request signal requesting <u>to acquire</u> a use of each of said unit data buses and to

<u>transfer data on</u> ~~use~~ said unit data buses requested when a request by means of said <u>bus</u>

request signal is granted; and

one bus controller connected to all of the bus masters and configured to split-control

said unit data buses for said plurality of bus masters by giving a grant signal to the bus

masters, which grants the use of each of said unit data buses in accordance with said <u>bus</u>

request signal, wherein

the <u>bus</u> request signal <u>is sent to said bus controller prior to data transfer and</u> has a field

comprising a plurality of bits <u>for specifying necessary bit width</u>, each of which said plurality

of bits <u>identifying</u> ~~corresponding to~~ respective one of said unit data buses, and said bus

controller grants the use of each of said unit data buses specified by the bits of said <u>bus</u>

request signal.

Claim 9 (Previously Presented): The information processing system according to

claim 8, wherein:

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said bus controller sends the grant signal to said bus masters based on a bus release

requesting signal requesting a release of said unit data buses.

Claim 10 (Previously Presented): The information processing system according to

claim 8, wherein:

said bus controller includes a monitor circuit for monitoring availability of said unit

data buses.

Claim 11 (Previously Presented): The information processing system according to

claim 10, wherein:

said bus controller judges whether said unit data buses of said data bus are available

based on a monitoring result of said monitor circuit, and when said unit data buses are

available, said bus controller gives the grant signal of the use of said unit data buses to said

bus master.

Claim 12 (Previously Presented): The information processing system according to

claim 10, wherein:

said bus controller sends a state signal indicating the availability of said unit data

buses to each of said bus masters based on a monitoring result of said monitor circuit.

Claim 13 (Currently Amended): The information processing system according to

claim 8, wherein:

said bus request signal includes information specifying each unit data bus in said data

bus.

Claim 14 (Currently Amended): The information processing system according to claim 8, wherein:

said bus request signal includes information specifying the number of the unit data buses in said data bus.

Claim 15 (Currently Amended) A method of carrying out data transfer through a data bus having a plurality of unit data buses by using a plurality of bus masters, comprising:

generating a bus request signal requesting to acquire a use of each of unit data buses in each of a plurality of bus masters connected to each of the unit data buses and sending said each bus request signal to a bus controller connected to all of the bus masters prior to data transfer, said data bus being connected to a peripheral apparatus and each of said unit data buses transfers data concurrently;

sending, in response to said bus request signal, a grant signal granting the use of each of said unit data buses to the bus masters in accordance with said bus request signal; and

occupying said unit data buses granted by said grant signal, and carrying out data transfer by using the unit data buses thus occupied, wherein

the bus request signal has a field comprising a plurality of bits for specifying necessart bit width, each of said plurality of bits identifying corresponding to a respective one of said unit data buses, and said bus controller grants the use of each of said unit data buses specified by the bits of said bus request signal.

Claim 16 (Previously Presented): The method according to claim 15, wherein:

sending of said grant signal includes sending said grant signal based on a bus release requesting signal requesting a release of said unit data buses.

Claim 17 (Previously Presented): The method according to claim 15, further comprising:

monitoring availability of said unit data buses.

Claim 18 (Previously Presented): The method according to claim 17, wherein:

sending of said grant signal includes sending the grant signal based on the availability of said unit data buses.

Claim 19 (Previously Presented): The method according to claim 17, further comprising:

sending a state signal indicating the availability of said unit data buses to each of said bus masters.

Claim 20 (Currently Amended): The method according to claim 15, wherein:

generating of said bus request signal includes generating said bus request signal including-information specifying each unit data bus in said data bus or information specifying the number of the unit data buses in said data bus.

Claim 21 (Currently Amended) A data transfer control circuit for carrying out data transfer by using a plurality of bus masters, comprising:

a data bus connected to a peripheral apparatus, said data bus having a plurality of unit data buses, each of which transfers data concurrently;

a plurality of bus masters connected to each of the unit data buses and configured to send a bus request signal requesting to acquire a use of each of said unit data buses and to

transfer data on ~~use~~ said unit data buses requested in response to a bus master select signal which indicates the current bus master to which said grant signal is given; and

one bus controller connected to all of the bus masters and configured to split-control said unit data buses for said plurality of bus masters by giving a grant signal to the bus masters, which grants the use of each of said unit data bus in accordance with said <u>bus</u> request signal, and sending said bus master select signal to each of said bus masters, wherein the request signal <u>is sent to said bus controller prior to data transfer</u> has a field comprising a plurality of bits <u>for specifying necessary bit width</u>, each of said plurality of bits <u>identifying</u> ~~corresponding to~~ a respective one of said unit data buses, and said bus controller grants the use of each of said unit buses specified by the bits of said <u>bus</u> request signal.

Claim 22 (Currently Amended) An information processing system for carrying out data transfer by using a plurality of bus masters, comprising:

a peripheral apparatus;

a data bus connected to a peripheral apparatus, said data bus having a plurality of unit data buses, each of which transfers data concurrently;

a plurality of bus masters connected to each of the unit data buses and configured to send a <u>bus</u> request signal requesting <u>to acquire</u> a use of each of said unit data buses and to transfer data on ~~use~~ said unit data buses requested in response to a bus master select signal which indicates the current bus master to which said grant signal is given; and

one bus controller connected to all of the bus masters and configured to split-control said unit data buses for said plurality of bus masters by giving a grant signal to the bus masters, which grants the use of each of said unit data buses in accordance with said <u>bus</u> request signal, and sending said bus master select signal to each of said bus masters, wherein

the request signal <u>is sent to said bus controller prior to data transfer and</u> has a field comprising a plurality of bits, each of said plurality of bits corresponding to a respective one of said unit data buses <u>for specifying necessary bit width</u>, and said bus controller grants the use of each of said unit buses specified by the bits of said <u>bus</u> request signal.

Claim 23 (Currently Amended) A method of carrying out data transfer through a data bus having a plurality of unit data buses by using a plurality of bus masters, comprising:

generating a <u>bus</u> request signal requesting <u>to acquire</u> a use of each of unit data buses in each of a plurality of bus masters connected to each of the unit data buses and sending, in response to a bus master select signal which indicates the current bus master to which said grant signal is given, said each <u>bus</u> request signal to a bus controller connected to all of the bus masters <u>prior to data transfer</u>, said data bus being connected to a peripheral apparatus and each of said unit data buses transferring data concurrently;

sending, in response to said <u>bus</u> request signal, a grant signal granting the use of each of said unit data buses to the bus masters in accordance with said <u>bus</u> request signal, and sending said bus master select signal to each of said bus masters; and

occupying said unit data buses granted by said grant signal, and carrying out data transfer by using the unit data buses thus occupied, wherein

the request signal has a field comprising a plurality of bits <u>for specifying necessary but width</u>, each of said plurality of bits <u>identifying</u> ~~corresponding to~~ a respective one of said unit data buses, and said bus controller grants the use of each of said unit buses specified by the bits of said <u>bus</u> request signal.

Claim 24-26 (Cancelled).

Claim 27 (Previously Presented) The data transfer control circuit according to claim 1, wherein

said bus controller broadcasts a bus master selection signal to all of said bus masters along with said grant signal, said selection signal indicating a bus master by which said grant signal is to be received.

Claim 28 (Previously Presented) The information processing system according to claim 8, wherein said bus controller broadcasts a bus master selection signal to all of said bus masters along with said grant signal, said selection signal indicating a bus master by which said grant signal is to be received.

Claim 29. (Currently Amended) A data transfer control circuit for carrying out data transfer by using a plurality of bus masters, comprising:

a data bus connected to a peripheral apparatus, said data bus having a plurality of unit data buses, each of which transfers data concurrently;

a plurality of bus masters connected to each of the unit data buses and configured to send a <u>bus</u> request signal requesting <u>to acquire</u> a use of each of said unit data buses <u>prior to data transfer</u>, and to <u>transfer data on</u> <s>use</s> said unit data buses requested when a request by means of said <u>bus</u> request signal is granted; and

one bus controller connected to all of the bus masters and configured to split-control said unit data buses for said plurality of bus masters by giving a grant signal to the bus masters, which grants the use of each of said unit data buses in accordance with said <u>bus</u> request signal, wherein

the request signal has a field comprising a plurality of bits, each of said plurality of bits <u>identifying</u> <s>corresponding to</s> a respective one of said unit data buses, and

said bus master sends the <u>bus</u> request signal to another bus master and the bus

controller, and the other bus master determines the availability of each of the unit data buses

based on the <u>bus</u> request signal to send the <u>bus</u> request signal specifying available unit data

bus.